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# Cisco Silicon One Q200 and Q200L Processors

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The silicon industry has always been plagued with the trichotomy of switching silicon, routing line card silicon, and routing fabric silicon. Using these three basic building blocks, silicon and system vendors created unique architectures tuned for individual markets and industries. Consequentially, forcing customers to consume and manage these disjointed and dissimilar products caused an explosion in complexity, CapEx, and OpEx for the industry.

The Cisco Silicon One™ architecture ushers in a new era of networking, enabling one silicon architecture to address a broad market space, while simultaneously providing best-of-breed devices.

At 12.8 Tbps, the Cisco Silicon One Q200 builds on the ground-breaking technology of the Cisco Silicon One Q100 device, increasing the lead over all other routing silicon in the market. The Q200 is one of the highest bandwidth, highest performance, most flexible, and most power-efficient routing silicon on the market.

At 12.8 Tbps, the Cisco Silicon One Q200L extends the Cisco Silicon One family into the web-scale switching market offering one of industry's highest performance, most flexible, and most power-efficient 12.8 Tbps switching silicon on the market.

## Product overview

The Cisco Silicon One Q200 processor is a 12.8-Tbps, full-duplex, routing processor with deep buffers, while the Q200L is a 12.8-Tbps, full-duplex, switching processor. These processors can be configured in one of the following modes:

- Q200
  - 12.8-Tbps, full-duplex, standalone routing processor with deep buffers
  - 6.4-Tbps, full-duplex line card routing processor with deep buffers
- Q200L
  - 12.8-Tbps, full-duplex, standalone switching processor
  - 12.8-Tbps, full-duplex fabric element
  - 6.4-Tbps, full-duplex line card switching processor

Cisco Silicon One Q200 and Q200L can be used to build a wide range of products covering fixed form factor routers and switches, modular chassis routers and switches, and multipetabit disaggregated routers and switches.

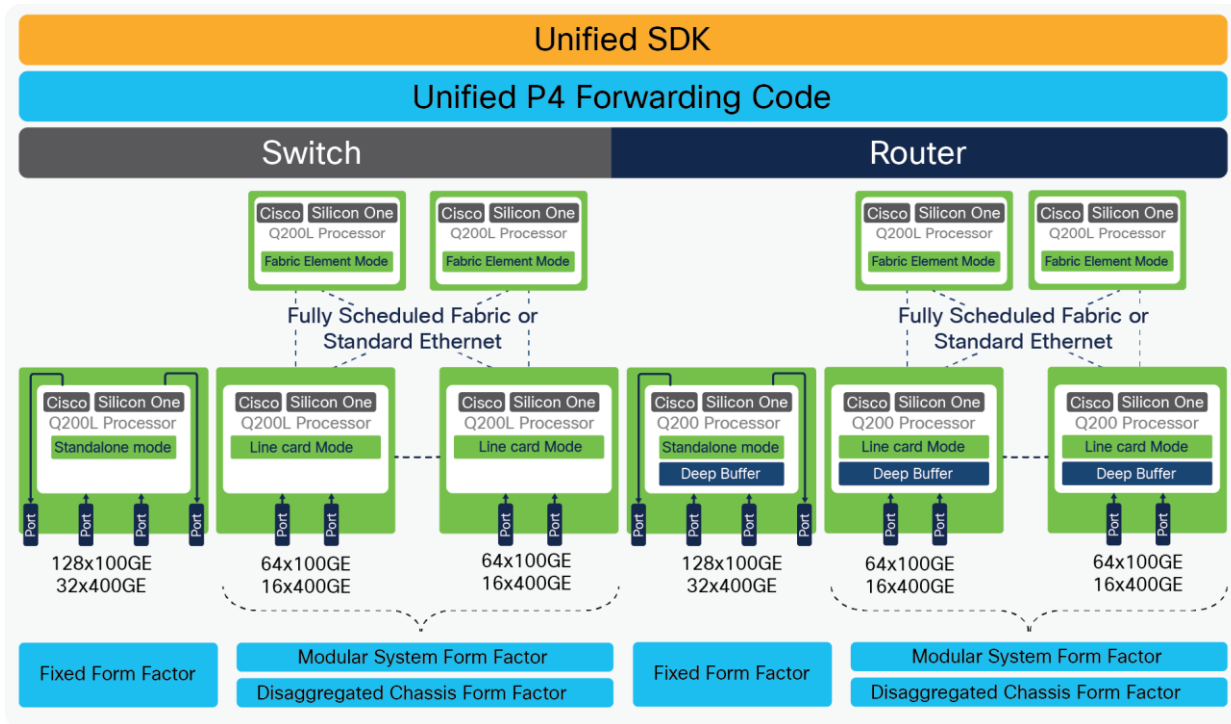


Figure 1.  
Form factors

## Features and benefits

Table 1. Architectural Characteristics and Benefits

Feature	Benefit
Unified architecture across multiple markets	Greatly simplifies customer network infrastructure deployments
Unified SDK across market segments and applications	Provides a consistent point of integration for all applications across the entire network infrastructure
High-bandwidth routing and fabric silicon	7-nm, 12.8-Tbps routing, switching, and fabric silicon
High-performance routing and switching silicon	Achieve line rate at small packet sizes
Power-efficient routing and switching silicon	The power efficiency of 7 nm and the Cisco Silicon One architecture
Large and fully unified packet buffer	Fully shared on-die buffer with optional, large external packet buffer
Switching efficiency with routing features and scale	Addresses the requirements of service provider and web-scale providers' routing and switching applications
Run-to-completion network processor	Provides feature flexibility without compromising performance or power efficiency
P4 programmable	Leverages an open-source programming language to enable customers to define their own features

## Prominent feature

### Flexibility, Performance, and Scale for Next-Generation Service Provider and Web-Scale Networks

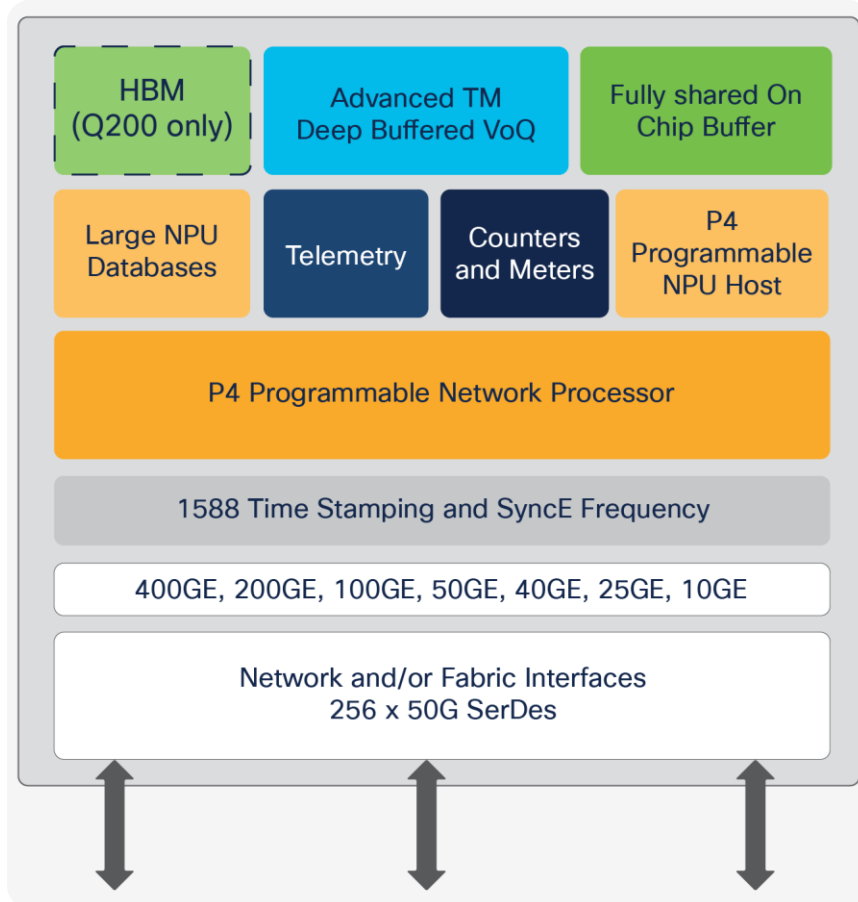


Figure 2.  
Block Diagram

### Features

- 256 56G SerDes; each can be configured independently to operate in 10G/25G/50G using NRZ or PAM4 modulation
- Flexible port configuration supporting 10/25/40/50/100/200/400 Gbps
- Large, fully shared, on-die packet buffer
- Large, in-package packet buffer (Q200 only)
- 1588v2 and SyncE support with nanosecond-level accuracy

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- On-chip, high-performance, P4-programmable host NPU for high-bandwidth offline packet processing (for example, OAM processing, MAC learning)
  - Multiple embedded processors for CPU offloading

### Traffic Management

- Large pool of configurable queues, supporting DiffServ and hierarchical QoS
- Support for system-level, end-to-end QoS and scheduling for both unicast and multicast traffic
- Seamless extension of on-die buffer to external packet buffer
- Support for ingress and egress traffic mirroring
- Support for link-level (IEEE802.3x), PFC priority-level (802.1Qbb) flow control and ECN Marking
- Support of port extenders

### Network Processor

- Run-to-completion, P4-programmable network processor
- Line rate at very small packets even with complex packet processing
- Large and shared fungible tables
- Support for complex packet processing features without impacting data rate
- Support for simple packet processing features with optimized power and latency

### Load Balancing

- Flow load balancing using ECMP or LAG
- Dynamic flowlet load balancing with ability to detect and handle elephant flows
- Packet-by-packet load balancing, creating an optimal, flow-independent, end-to-end scheduled and lossless fabric

### Instrumentation and Telemetry

- Programmable meters used for traffic policing and coloring
- Programmable counters used for flow statistics and OAM loss measurements
- Programmable counters used for port utilization, microburst detection, delay measurements, flow tracking, elephant flow detection, and congestion tracking
- Traffic mirroring: (ER)SPAN on drop
- Support for sFlow and NetFlow

### SDK

- APIs provided in both C++ and Python
- Configurability via high-level networking objects
- Distribution-independent Linux packaging

- Robust simulation environment enables rapid feature development
- CPU packet I/O through native Linux network interfaces

#### P4 Programmability

- Application development is handled by a P4-based IDE programming environment
- At compilation, the P4 application generates low-level register/memory access APIs and higher-level SDK Application APIs
- Provides application support for a wide range of data center, service provider, and enterprise protocols
- Modifications to the provided application can be easily accomplished using the provided P4 development environment
- Ability to develop the SDK and applications running over the SDK over a simulated Cisco Silicon One device

#### Cisco P4 Application

Due to Silicon One’s extensible P4 programming toolkit, we are always adding features to address new markets and new customer requirements; however, a sample of the features that are currently available with the P4 code is provided below:

<ul style="list-style-type: none"> <li>• IPv4/v6 Routing               <ul style="list-style-type: none"> <li>◦ OSPF</li> <li>◦ IS-IS</li> <li>◦ BGP</li> </ul> </li> <li>• MPLS Forwarding               <ul style="list-style-type: none"> <li>◦ LDP, LDPoTE</li> <li>◦ RSVP-TE</li> <li>◦ SR-MPLS</li> <li>◦ SR-TE</li> <li>◦ L3VPN, 6PE, 6VPE</li> <li>◦ BGP LU</li> <li>◦ VPWS/EoMPLS</li> <li>◦ VPLS</li> </ul> </li> <li>• Ethernet Switching               <ul style="list-style-type: none"> <li>◦ 802.1d, 802.1p, 802.1q, 802.1ad</li> </ul> </li> <li>• IP Tunneling               <ul style="list-style-type: none"> <li>◦ IPinIP</li> <li>◦ GRE</li> <li>◦ VXLAN</li> </ul> </li> <li>• Integrated Routing and Bridging (IRB)</li> <li>• HSRP/VRRP</li> <li>• Policy-Based Routing</li> <li>• Security and QoS ACLs</li> </ul>	<ul style="list-style-type: none"> <li>• ECMP and LAG (802.3ad)</li> <li>• Multicast               <ul style="list-style-type: none"> <li>◦ PIM-SM/SSM</li> <li>◦ IGMP</li> <li>◦ MLDP</li> <li>◦ MVPN</li> </ul> </li> <li>• NAT/PAT</li> <li>• Protection (Link/Node/Path and TI-LFA)</li> <li>• QoS Classification and Marking</li> <li>• Congestion Management</li> <li>• Telemetry               <ul style="list-style-type: none"> <li>◦ NetFlow, sFlow</li> <li>◦ (ER)SPAN</li> <li>◦ Packet Mirroring with Appended Metadata</li> <li>◦ Lawful Intercept</li> </ul> </li> <li>• DDoS Mitigation               <ul style="list-style-type: none"> <li>◦ Control-Plane Policing</li> <li>◦ BGP Flowspec</li> </ul> </li> <li>• Timing and Frequency Synchronization               <ul style="list-style-type: none"> <li>◦ SyncE</li> <li>◦ 1588</li> </ul> </li> </ul>
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## Product Sustainability

Information about Cisco's environmental, social, and governance (ESG) initiatives and performance is provided in Cisco's CSR and sustainability [reporting](#).

**Table 2.** Cisco Environmental Sustainability Information

Sustainability Topic		Reference
General	Information on product-material-content laws and regulations	<a href="#">Materials</a>
	Information on electronic waste laws and regulations, including our products, batteries, and packaging	<a href="#">WEEE Compliance</a>
	Information on product takeback and reuse program	<a href="#">Cisco Takeback and Reuse Program</a>
	Sustainability inquiries	Contact: <a href="mailto:csr_inquiries@cisco.com">csr_inquiries@cisco.com</a>
Material	Product packaging weight and materials	Contact: <a href="mailto:environment@cisco.com">environment@cisco.com</a>

## For more information

[Learn more](#) about the Cisco Silicon One

**Americas Headquarters**  
Cisco Systems, Inc.  
San Jose, CA

**Asia Pacific Headquarters**  
Cisco Systems (USA) Pte. Ltd.  
Singapore

**Europe Headquarters**  
Cisco Systems International BV Amsterdam,  
The Netherlands

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